Amendment to the Specification

Replace the existing paragraph [0033] with the following paragraph [0033]:

[0033] The AGD calculator may also correct errors in the output signals of the FFT decoding circuit 310 in response to the phase error signals contained therein. The AGD calculator uses a phasor to estimate the average delay of a multi-carrier modulation symbol. The AGD calculator 310 translates the phasor to a timing offset and feeds back the timing offset back to the symbol clock generating circuit 314 which in turn feeds the timing offset back to the demodulator 301 in receiver 302. It should be noted that the timimg offset can be directly determined from the OFDM symbols using a discriminator 311 in the feedback loop. The AGD calculator 310 is followed by a parallel-to-serial (P/S) converter 312. The output signals of the AGD calculator 310 (that is, the error-correction-resultant signals) are subjected by the P/S converter 312 to parallel-to-serial (P/S) conversion, being thereby rearranged and combined into a serial-form digital signal. The P/S converter 312 operates in response to a clock signal fed from a clock signal generating circuit in the symbol clock generating circuit 314. The serial-form digital signal is transmitted from the P/S converter 312 to an external device (not shown).